POWER MOS ARRAYS WITH NON-UNIFORM POLYGATE LENGTH

Field of the Invention

The invention relates to the field of power MOS arrays. In particular it relates to a new MOS array structure.

Background of the Invention

For high power applications, e.g. for powering large microprocessors that operate at 2V and sink approximately 50 A, single semiconductor devices are typically inadequate to provide the requisite power. Power transistors in the form of arrays of transistors are commonly used. These comprise arrays of transistors connected in parallel. Figure 1 shows a plan view of a typical rectangular array 100 of NMOS devices. Each polygate 102 supports a plurality of drains and sources (not shown) to define a plurality of NMOS transistors. For each polygage, the drains and sources are typically arranged as opposed, staggered, comb-like structures to define alternating drains and sources extending along both sides of the polygate for the width of the polygate 100.

Array structures are also formed from other devices such as LDMOS, but due to the octagonal configuration of LDMOS devices, such arrays typically have a honeycomb-like layout.

Summary of the Invention

The present invention comprises a power MOS array having at least one polygate supporting a plurality of sources and drains connected in parallel, wherein the polygate has a non-uniform length along its width. Typically the array includes a common drain interconnect and a common source interconnect. The drain and source interconnects may have a comb-like configuration. Preferably drain and source interconnects are opposed and staggered to define an alternating drain and source regions on either side of the polygate and extending substantially along the width of the polygate. The drain interconnect and source interconnect may each have at least one metal contact with the length of the polygate being shorter at greater distances from the at least one contact. The

array may, for example, have only one drain contact and one source contact if the drain and source regions do not alternate. Instead there may be a drain contact on each side of the polygate and a source contact on each side of the polygate if the drain and source regions are staggered. Each drain contact may be in the middle of a drain interconnect and each source contact may be in the middle of a source interconnect. The polygate in such an embodiment typically is longer in the middle and gets shorter towards the ends. The change in length of the polygate may be non-linear. Preferably the decrease in length of the polygate further away from the drain and source contacts corresponds to the increase in resistance along the interconnect as one moves further from the drain and source contacts.

Brief Description of the Drawings

Figure 1 shows a plan view of a prior art power MOS array.

Figure 2 is a schematic representation of part of the array of Figure 1;

Figure 3 shows a simple prior art power MOS array having a single polygate;

Figure 4 shows a simple power MOS array of the invention having a single polygate of non-uniform length,

Figure 5 shows a voltage distribution curve along the length of the drain interconnect of the prior art array of Figure 3, and

Figure 6 shows the polygate structure defined based on the current distribution of Figure 5.

Detailed Description of the Invention

In order to best understand the present invention it is useful to consider again the prior art array shown in Figures 1 as well as the prior art depictions in Figures 2 and 3. The array 100 shows 12 polysilicon gates 102 extending from one end 104 to the other 106. The location of the source contact and the drain contact are shown by reference numerals 110 and 112 , although the contacts are not actually shown in Figure 1. Although not shown, in order to connect the MOS devices of the array in parallel, comb-like interconnects

extend from one end 104 to the other end 106 for each of a plurality of drains and sources that are spaced along the width W of each polysilicon gate 102.

The principle of connecting numerous transistors in parallel in order to handle the high power current requirements is best illustrated in the schematic circuit diagram of Figure 2, which shows three NMOS transistors with their gates 200 connected in parallel. In practice the plurality of transistors are simply produced with a common polygate as shown in Figures 1 and 3.

Figure 3 shows an array 300 with a single polysilicon gate 302. A plurality of sources 304 and a plurality of drains 306 are shown extending along the width W of the polysilicon gate 302. As shown in Figure 3, the source interconnects 310 and drain interconnects 312 are formed into comb-like structures by two different metal layers. The comb-like structures in this embodiment are staggered to provide alternating drain and silicon regions along both sides of the polygate 302. As in the embodiment of Figure 1, there is only one source contact 320 on each side of the polygate 302, for the source interconnects 310, and one drain contact (not shown because it is to the lower metal interconnect layer) on each side of the polygate 302, for the drain interconnects. Thus, the current supplied to the drain contact will experience a resistance presented by the drain interconnect which gets progressively larger the further one moves from the drain contact. Similarly current experiences an increasing resistance as the distance from the source contact 320 increases. Thus the drain regions 306 and source regions 304 that are further from the center of the structure 300 (where the drain and source contacts are) will receive less current. This is illustrated in Figure 1 by the wider arrow 120 in the middle of the structure, and the narrower arrows 122 toward the ends 104, 106. It should be noted that the gate length remains unvaried at L, along its entire width W.

The present invention compensates for this current loss by providing for reduced polygate impedance as one moves further away from the center of the structure 300. This is done by reducing the length L of the polygate as one moves toward the ends of the array structure.

This is illustrated in Figure 4, which shows the polygate 400 getting shorter (reduced length L) as one moves away from the center toward the ends 402, 404.

While some embodiments have used a linear decrease in polygate length, a non-linear decrease as shown in Figure 4 is preferable. Ideally the reduction in polygate length should be a function of the increase in resistance through the drain and source interconnects as one moves further away from the drain and source contacts.

Figure 5 shows a graph of voltage changes across the polygate as one moves from one end of the structure to the other. As can be seen the voltage is at a maximum at the center where contacts are, and drops off toward both ends due to a potential drop across the drain and source interconnects. Figure 6 shows a gate configuration that corresponds in length at the various locations along its width, to the voltage that would exist across the polygate if the polygate length were not adjusted.

It will be appreciated that the relationship between the voltage change and an unaltered device and the polygate length change that is required to compensate for the voltage change, can be determined in a number of ways. For example, the voltage can be measure at various locations along the width of an unaltered device and the length of the polygate adjusted accordingly to achieve the corresponding reduction in resistance across the polygate to compensate for the decrease in voltage at each measured location. Instead simulation results can be used to design the ideal polygate configuration.

The effect of compensating for the voltage reduction further away from the drain and source contacts, is that the array works more efficiently by fully utilizing each transistor in the array. However, optimization of the polygate length change, e.g., by extraction and simulation is important to ensure that transistor leakage and hot electron boundary considerations are not violated by making the polygate too short.

While the present invention was described specifically for rectangular NMOS arrays, it will be appreciated that similar benefits can be achieved with other power MOS arrays, such as a honeycomb-like arrays of LDMOS devices.